Bus Currents and Voltages when operating a Modular Multilevel Converter (M2LC) in Resonance Mode

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Revision -

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Revision – (9/21/18) First draft.

Abstract

The discussion of a proposed technique to produce DC or low frequency AD at the output of a *multilevel converter* (M2LC) was presented in Operation of M2LC in Resonance Mode.

The paper presented a simulation of one leg of a M2LC stack operating in a special mode that would force a resonance condition based on the values of the interphase inductance and link capacitor selected. The cited paper also presented operation of one M2LC stack under various load conditions.

In all simulations presented, the plus and minus bus was presented as a zero impedance volage set at fixed +/- 1000 volts DC of zero impedence. In reality, the implementation of a high voltage M2LC would not provide for an ideal condition such as this.

Any references to the operattion of a mult-phase configuration of the stack (say 3-phase) presented in the cited paper was created by superimposing seperate operating conditions for each phase. For example, one sumulation presented was an operating condition where Phase-A was connected to a +20 amp current source, and Phase-C was connected to a -20 amp current source (Phase-B was open). The resonance mode was set to *intermediate* (see Figure 43 of Operation of M2LC in Resonance Mode).

The purpose of this paper, is to gain some insight into the operation of a 3-phase M2LC in renonance mode, under a more realistic condition where impedance is present in both the plus and minus bus connections.

Background

The diagram for the circuit used in this presentation is shown in Figure 1.

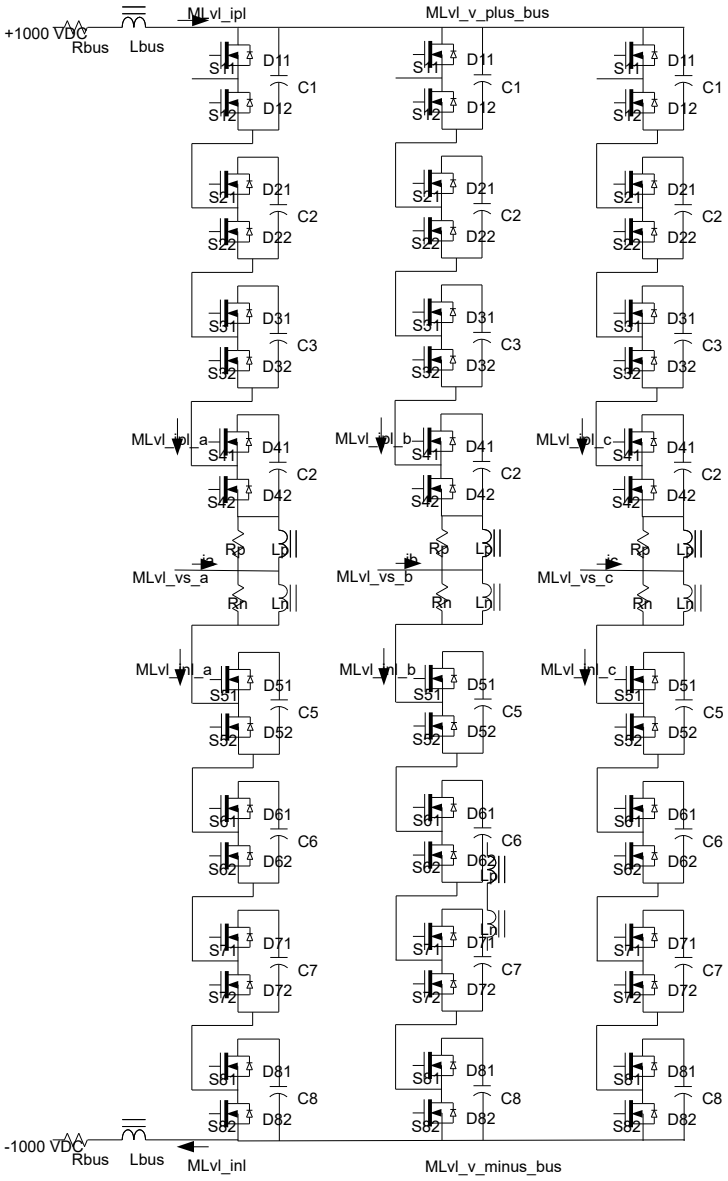

Figure 1 Diagram of the circuit used in this simulation.

Rbus	.001 ohms
Lbus	.25 mH

The characteristics of each of the three M2LC stacks is identical to that presented in Figure 1 of Operation of M2LC in Resonance Mode. However as shown here, three phases are connected to a common + and – DC bus with series impedance.

In Operation of M2LC in Resonance Mode, the single M2LC stack was simulated using a fixed time step of .00000064 seconds applied to 68 x 68 matrix. For this simulation, the addition of a concurrent operation of three phase using a single step calculation would involve a matrix size greater then 3*68 x 3*68. Using this type of approach like would be prohibitive to say the least.

Instead, I choose a simpler method using two time steps per calculation. This is outlined in Figure 2.

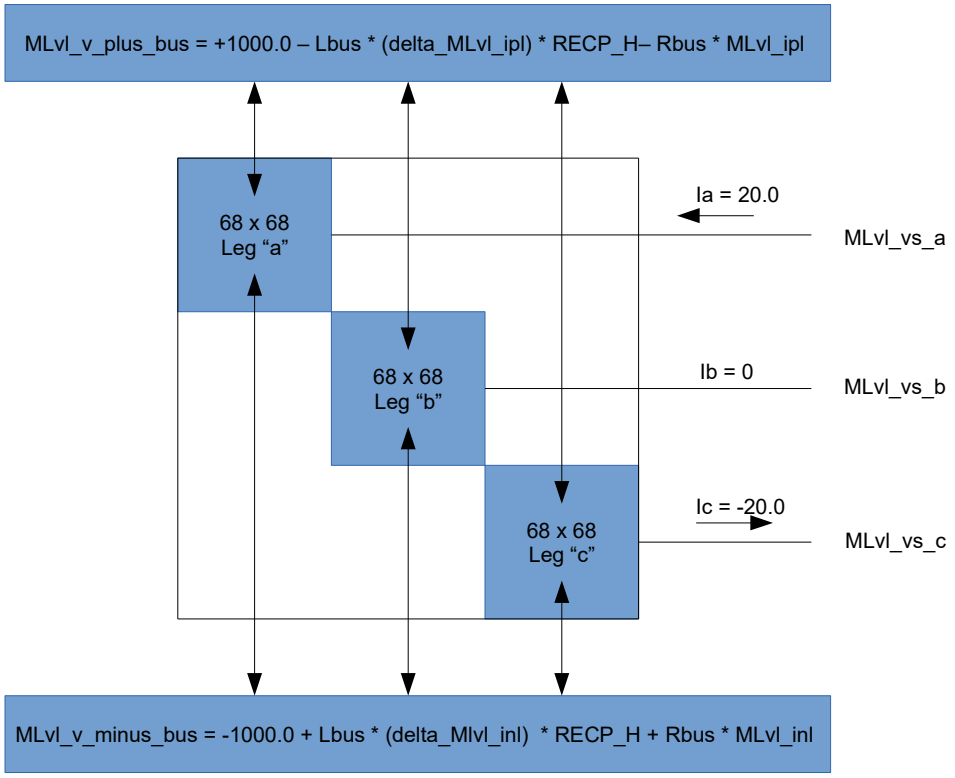

Figure 2 Block diagram of method to determine the plus and minus bus voltages labeled **MLvl_v_plus** and **MLvl_v_minus_bus**.

The simulation represented in Figure 2 is accomplished by *forking* three processes in Linux, one process for each 68 x 68 matrix describing the M2LC stack representing the legs of phases A, B, and C. Process number 1 (phase A) is set for the desired switching sequence with a +20 amp current source applied to the load connection (in this case **MLvl_vs_a**). A similar setup is done for process 2 (phase B) and process 3 (phase C). Note that the system is balanced (20 amps in and 20 amps out at the load connections).

All three processes are run for one time step wih H = .00000064 seconds, with RECP_H equal to 1/H as shown in Figure 2. Then the bus plus and minus *leg* currents of all three stacks (labeled **MLvl_ipl_<leg>** and **MLvl_inl_<leg>** in Figure 1) are added to determine **MLvl_ipl** and **MLvl_inl** in Figure 2. From this information, the second step in executed (in the same time step) to detemine **MLvl_v_plus_bus** and **MLvl_v_minus_bus**. The values **MLvl_v_plus_bus** and **MLvl_v_minus_bus**

are then fed back to each of the three processes in order calculate the states for the next time step.

The modulation sequences for each stack (phase) as viewed form the load connections **MLvl_vs_a, MLvl_vs_b** and **MLvl_vs_c** are shown in Figure 3.

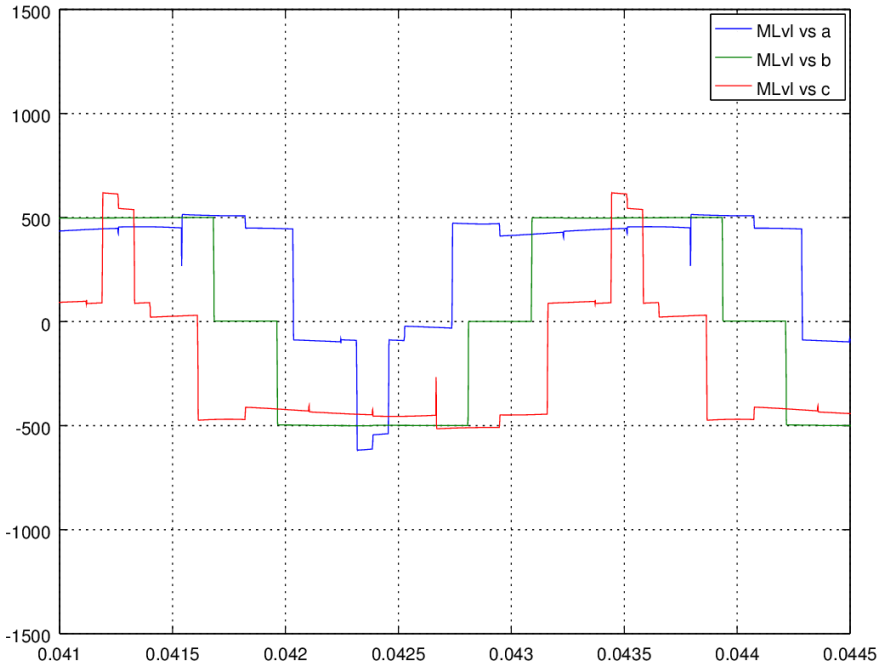

Figure 3 Modulation sequences viewed at load connections.

The resulting bus voltages and currents are shown in Figure 4 and Figure 5 respectively. The system is balanced as evident in Figure 5 where the current flowing in the plus bus is equal to the current flowing in the minus bus.

The discontinuities of the bus voltages shown in Figure 4 are due in part to simulation noise and the points where the change in bus current goes to zero due to short intervals where current *circulation* within the 3-phase bridge occures.

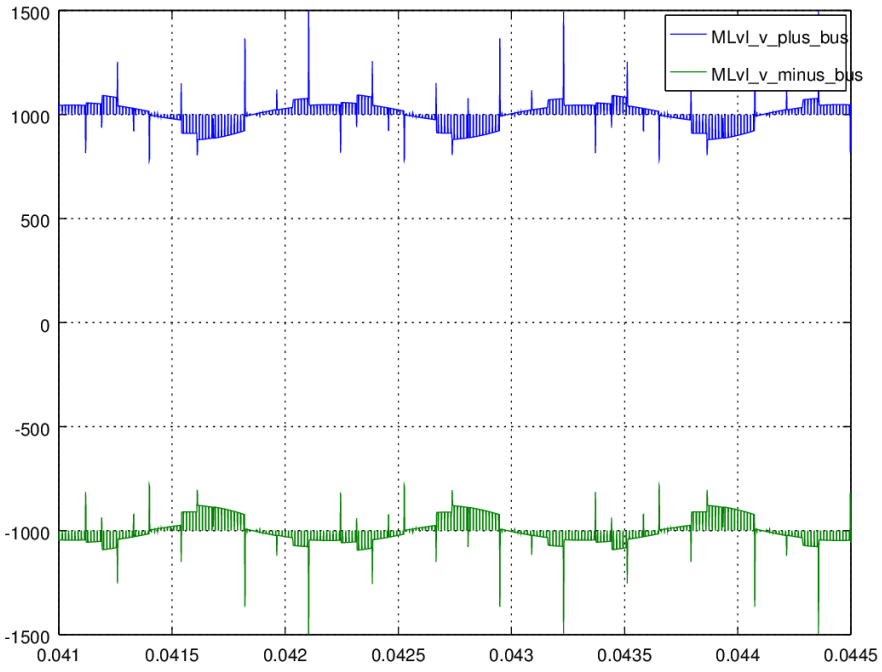

Figure 4 Simulated bus voltages for the system depected in Figure 1.

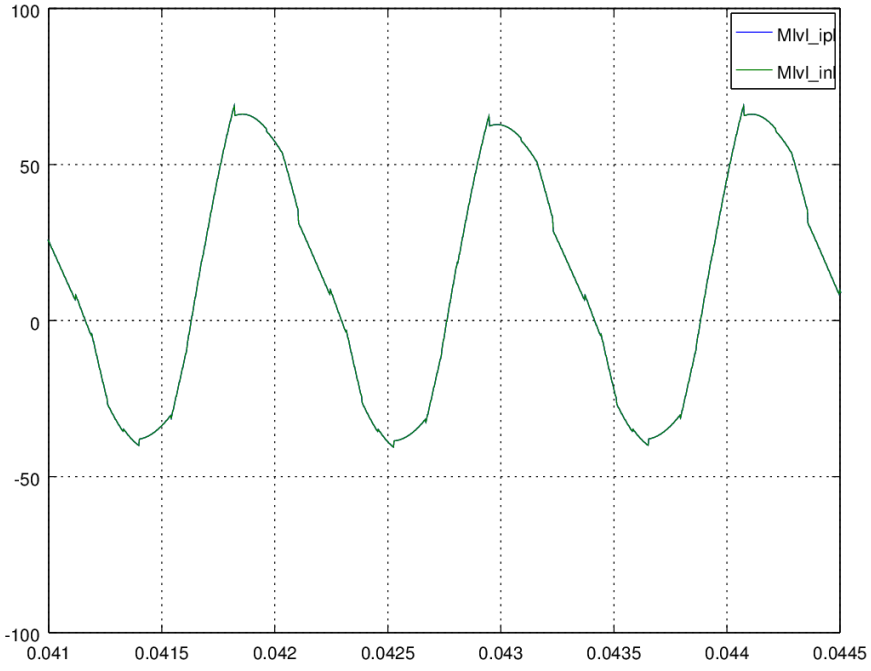

Figure 5 Simulated bus currents for the system depected in Figure 1.